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by

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Originally published by IEEE 67th Electronic Components and Technology Conference, Orlando, Florida, May 30 – June 2, 2017.

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Abstract— **With shrinking of chip sizes, Wafer Level Chip Scale Packaging (WLCSP) becomes an attractive and holistic packaging solutions with various advantages in comparison to conventional packages, such as Ball Grid Array (BGA) with flipchip or wirebonding. With the advancement of various fan-out (FO) WLPs, it has been proven to be a more optimal, low cost, integrated and reliable solution compared to fan-in WLP because of the greater design flexibility in having more input/output (I/O), improved mechanical and thermal performance. In addition, FO-WLP shows superior high-frequency electrical performance due to its shorter, finer and simpler interconnection scheme compared to flipchip packaging. eWLB (embedded wafer level BGA) is a type of FO-WLP that enables applications requiring smaller form factor, excellent thermal performance and thin package profiles and it has the potential to evolve into various configurations with proven yields and manufacturing experience based on more than 8 years of high volume manufacturing of over 1.5B unit shipment.**

This paper discusses the recent advancements in robust board level reliability performance of eWLB for automotive application, where a review of a Design of Experiment (DOE) study will demonstrate improved Temperature Cycle on Board (TCoB) reliability. Several DOE studies were planned and test vehicles were prepared with various variables, such as materials, redistribution layer (RDL) design, copper (Cu) and under bump metallurgy (UBM) thickness, and a printed circuit board (PCB) pad design. The final test vehicle passed over 1000 times temperature cycles (TC) with optimized design factors of these parametric studies and reliability tests. To investigate potential structural defects after the reliability test, both destructive analyses were performed under industry standard test conditions, Daisy chain test vehicles were used for TCoB reliability performance.

Keywords-component; FOWLP, eWLB, Automotive packaging, 77GHz ADAS packaging, Reliablity, Failure Analysis

I. INTRODUCTION

The packaging of semiconductor has a significant impact on the overall device performance. In terms of the performance, size and scalability, traditional packaging technologies are reaching their limits which are required to meet the needs of emerging applications. In the next 10 years, the automotive integrated circuit (IC) market will outgrow by two times the rest of the IC market. Market researchers predict that by 2025, automotive semiconductors will occupy more than 15% of the total semiconductor market worldwide.

Currently, 8000 electronic components are used for Audi A8 and over 2000 electronic parts are used in automobiles on average [1] with 80% of innovations in automotive technology coming from semiconductors.

In terms of performance, power consumption, integration and reliability at a required cost, current and future demands of automotive semiconductors are met by developing advanced silicon process technology, innovative packaging solutions based on chip and package co-design, low cost materials, reliable interconnect technologies, and advanced assembly and test manufacturing systems.

Emerging WLCSP market of Automotive Applications

Market trends as experienced by the end application drive the emergence and evolution of any package technology. Currently, the primary automotive packaging solution is leaded or laminate wirebonding which is more than 90% of the total packaging market.

The smallest possible package size is the Wafer Level Chip Scale Package (WLCSP), since the final package is no larger than the required circuit area. Since its introduction, WLCSP has experienced significant growth due to the small form factor, lower cost and high performance requirements of mobile and portable applications.

WLCSP and 77GHz radar sensors with FOWLP are already well adopted in the automotive market for cabin or infotainment and ADAS (automotive Driving Assistant System) safety [2,3]. The range of applications continues to expand with the ultimately larger wave in the development of next generation automotive capabilities, i.e. electrical vehicle (EV) and autonomous driving car. In the next 3-5 years, the market share of current WLCSP volume is expected to double. The car radar market is expected to grow 28% annually (2015-2022) and reach more than $200M in packaging and assembly.

2377-5726/17 $31.00 © 2017 IEEE
DOI 10.1109/ECTC.2017.194

Advanced Wafer-Level Technology: eWLB/FO-WLP for mmWave & Automotive Radar Applications

With Si-based front-end technologies showing improved performance, wireless systems at millimeter wave (mmWave) frequencies become more and more important [3-5]. Adaptive Cruise Control (ACC) radar system at 77 GHz [6, 7], point-to-point radio link at 60 GHz or high resolution radio imaging at 94 and 140 GHz [8] are just a few examples of applications observed for upcoming markets. The impact of packaging on the overall electrical performance of the IC becomes increasingly important with frequencies increasing beyond 10 GHz. Thus, for the crucial development of commercial mmWave applications, the availability of high performance packages for monolithic microwave integrated circuit (MMIC) is crucial.

A few approaches for mmWave packaging solutions have been studied and reported based on Rogers 4350 substrate (low-loss material) surface mount-type (SMT) package for 1-40 GHz applications [9] or 77 GHz ceramic SMT package using an electromagnetic coupling as second-level interconnects [10]. Since they use traditional conventional laminate-based packaging and integration solutions, the packages were expensive and big size.

A very promising solution for mmWave packaging is eWLB package technology [11, 12]. It is based on an embedded device technology with fan-out redistribution. The thin-film redistribution layer (RDL) of the eWLB enables very flexible and highly customizable package designs. The length of the redistribution lines is in the range of the die size.

eWLB can achieve minimum interconnection length and excellent electrical performance up to mmWave frequencies. The conversion gain and the noise figure of the mixer affect the performance of the overall system. Therefore, a high transmission performance of a mmWave signal is very important in the design of a package.

In a number of cases, eWLB achieved a 20~50% reduction in package size as compared to other packaging solutions and over 60% volume reduction because of its slim and smaller form factor. For radio frequency (RF) and high-frequency devices, eWLB showed less parasitic electrical interference, therefore, it also significantly improved overall device electrical performance. In one example, a 77GHz SiGe mixer packaged as an eWLB achieved excellent high-frequency electrical performance due to the small contact dimensions and short signal pathways or interconnection length, which decreased parasitic effects [13].

Below list is the main factor of why eWLB is promising and suitable packaging solution for mmWave device or high frequency applications compared to substrate or laminate-based packaging, such as flipchip or wirebonding.

- Interconnection length: eWLB enables integration where the distance has to be as short as possible (loss increase with distance) to minimise loss (assuming both technologies have the same material loss).
- Conductance loss: Plated Cu in organic substrate materials has large surface roughness because of its base materials roughness used to improve adhesion and plating process control. eWLB uses a thin-film fab process for seed-layer and a well-controlled Cu plating to achieve a smooth Cu RDL surface which is more effective for skin effect in high frequency ranges.
- Dielectric loss: Organic substrate materials have high losses in mmWave range and also heterogeneous material sets bring complexity in terms of electrical behaviors. eWLB has molding compound and low-loss dielectric materials; therefore, less dielectric loss would be achieved.
- Design flexibility: eWLB provides more design flexibility for less routing interference with fine line width (LW) and line spacing (LS) capability (less than 10/10um LW/LS).

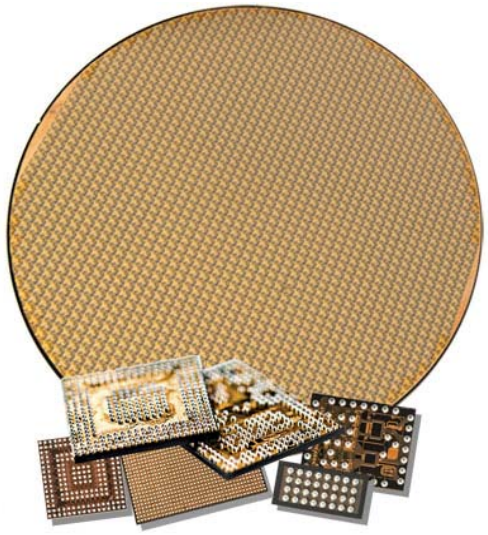


Figure 1. eWLB panel after RDL and ball drop and eWLB samples

Automotive radar technology is now facing a few changes of packaging, module assembly and manufacturing. Traditionally, bare die technology is used where the die is attached with adhesive to the printed circuit board (PCB) and electrical contact is performed by wire bonding on the board. This challenging assembly has to endure several critical process steps: from bare die handling to shaping wire bonds in a way that RF requirements are met[14].

One key element for the change from a quite complex and expensive solution to an easy-to-use and, therefore, inexpensive and affordable product is using standard surface

mount device (SMD) packaging technology. The eWLB package offers these properties and has been proven in a few mmWave applications.

This study focused on 2nd level reliability of the solder joint regarding temperature cycling as one of the major requirements of automotive applications, which requires a higher reliability spec of AEC (Automotive Electronics Council)-Q100 Grade-1. Thus, investigation and optimization of design factors, structure, process and material properties are of interest for eWLB packages develoopment. Comprehensive systematic design and structural parameter study and analysis were carried out to investigate and understand the TCoB reliability improvement of eWLB in harsh automotive conditions.

II. EXPERIMENTAL WORKS

Test Vehicle Specification

As mechanical test vehicle, eWLB package was designed in a 9x9mm package size and 0.5mm ball pitch and packaged with low temperature curable advanced dielectric materials, showing robust package reliability [15].

For the study of the Design of Experiment (DOE), several design factors such as PCB Cu landing pad structure, SMD (solder mask defined) or NSMD (nonsolder mask defined), solder mask opening diameter, Cu thickness in RDL layer, with or without UBM and a new solder alloy materials, were investigated. As per DOE, several different eWLB test vehicles were prepared accordingly.

Table 1. Test Vehicle Specification (DOE1 Reference).

Items	Specification
PKG size	9x9mm
Die Size	6x6mm
Ball Pitch	0.5mm
Ball Dia	0.3mm
IO No.	230
UBM	No
Cu RDL No.	1 layer
Die Thickness	440μm
PKG Thickness	770 μm

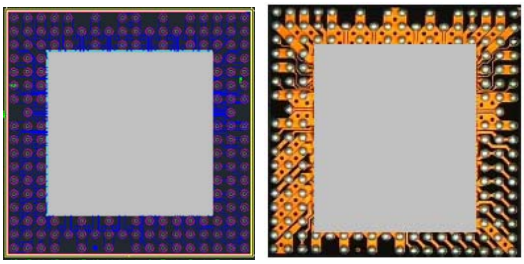


Figure 2. PKG drawing and micrograph of test vehicle of 9x9mm, 0.5mm pitch eWLB.

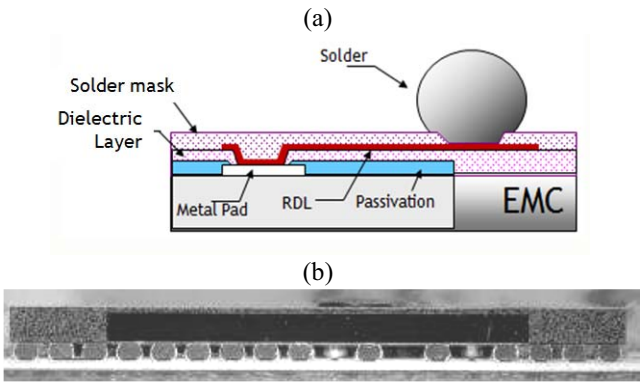


Figure 3. (a) stackup drawing of eWLB and (b) micrograph of cross-section of test vehicle as shown Table 1.

Component Level Reliability

For component level reliability tests, eWLB test vehicles were assembled and prepared. Table 2 shows the package level reliability test conditions in this study.

All tested eWLB test vehicles passed JEDEC standard package level reliability tests of AEC-Q100 Grade-1 successfully[16]. eWLB also passed JEDEC TC_B (-55/125ºC) and TC_C (-65/150ºC) conditions of temperature cycling test in this study.

Table 2. Package Level Reliability Results of eWLB with advanced dielectric material.

Test	Q100 Test Condition	Test Conditions
PC Pre-Cond	JEDEC J-STD-020	MSL1 24h bake @ 125°C 168h @ @ 85C/85%RH Reflow simulation (3times) with Lead free profile Tmax=260°C
THB Temp Humidity Bias	JESD22-A101/A110	Ta=85°C, 85%RH 1000h with bias
AC Auto-clave	JESD22-A102/A118	P=2.08atm Ta=121°C, 96h
TC Temp. Cycling	JESD22-A104	Ta = -55/+150°C 1000 cycles
PTC, Power Temperature Cycle	JESD22-A105	Ta = -50/+150°C 1000 cycles
HTSL, High Temp. Storage Life	JESD22-A103	Ta=150°C 1000h
THS, Temp Humidity Storage	JESD22-A101	Ta=85°C, 85%RH 1000h without bias
HAST Highly Accelerated	JESD22-A102/A118	130°C / 85% RH, no bias, 96hrs

Board Level Reliability

For board level reliability tests, eWLB test vehicles with a daisy chain connects were prepared and surface mounted on the PCB as illustrated in Fig. 4. To cover the most critical and important interconnections to investigate solder joint reliability effectively, this daisy chain connections in

the test vehicles were designed for various DOE samples of different eWLB designs were packaged and evaluated for TCoB board level reliability. Those daisychain test vehicles were tested in JEDEC TCoB condition (-40/125ºC, 2 cycles/hr). The PCB was prepared with RF materials in FR4 8-layer board of 1.2mm total PCB thickness. Cu pad diameter size was 250um and NSMD/SMD metal pads were prepared with an OSP surface finish. eWLB daisy chain test vehicles were attached on the PCB with solder paste for surface mounting. SMT assembly yield of over 99% was reported with solder paste printing. Then, the surface mounted boards were moved to the TCoB chamber with multi-channel event detector for on-line in-situ failure monitoring.

Table 3 illustrates TCoB board level reliability test results of DOE study of automotive eWLB packages.

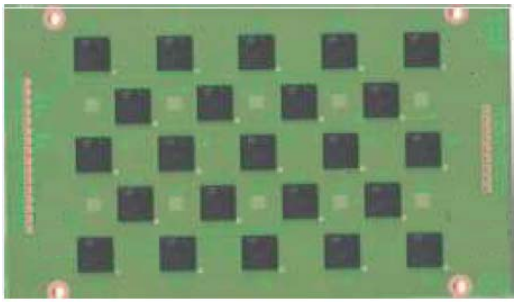


Figure 4. Micrograph of PCB for board level reliability with surface mounted eWLB packages.

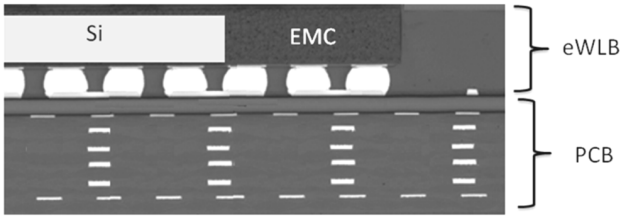


Figure 5. Micrograph of eWLB mounted PCB for board level reliability test.

The results from the DOE TCoB reliability studies are summarized as below:

1. NSMD board pads showed improved TCoB performance versus SMD ones in all DOE legs.
2. Larger solder mask opening was effective to improve results for the NSMD pad.
3. Thicker Cu RDL showed 15~20% improvement in TCoB test.
4. UBM did not effectively improve TCoB in this study, but is leading to big change in failure distribution. Need to further investigate and understand this behavior and failure mechanism(s).
5. With UBM and a new solder alloy B, it increased TCoB in NSMD pad.

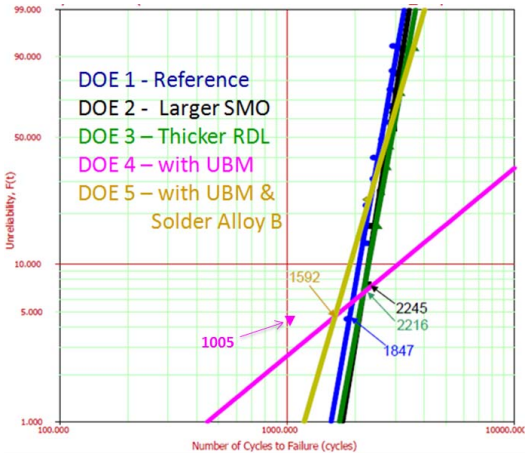


Figure 6. DOE study result : Weibull plot of TCoB reliability test with NSMD PCB. Each no. indicates the first failure cycle in each DOE studies.

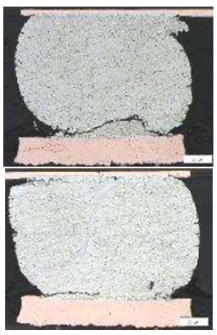
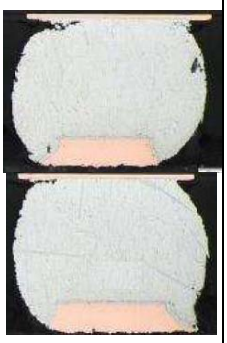
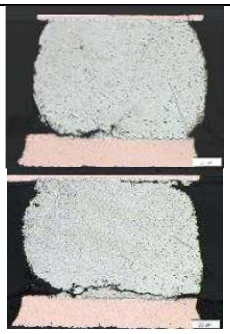
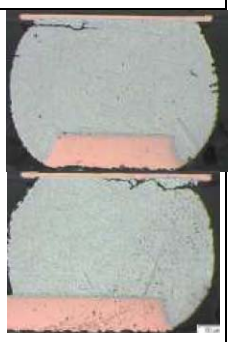
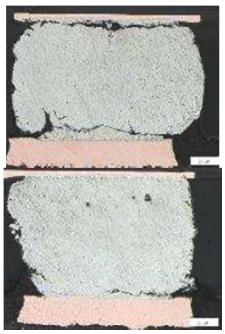
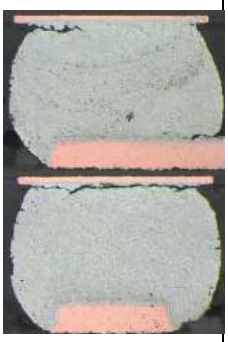
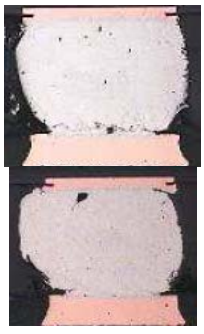
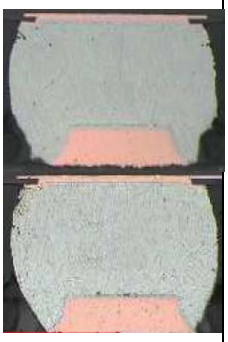
Table 3. Summary of TCoB reliability test results of DOE studies.

		First Failure Cycles	
		SMD	NSMD
DOE1	Reference	1452	1847
DOE2	Larger solder mask opening	1388	2245
DOE3	Thicker RDL	1763	2216
DOE4	With UBM+RDL	964	1005
DOE5	With UBM and Solder Alloy B	1002	1592

Failure Analysis of Solder Joint Reliability

After board level reliability tests, failure analysis was carried out to study solder joint fracture mode for each DOE case above mentioned. As shown Figure 7, optical micrographs show failure of SMD and NSMD samples, respectively.

SMD pad design leads to major failures at PCB pad side or to a combination with failures also at the package pad. But NSMD samples showed the only failure was on the package side and no PCB pad failure was observed. It means NSMD has good adhesion with a larger pad area, therefore thermomechanical stress is accumulated and focused on the package side. The DOE2 with a larger solder mask opening has improved solder joint life with larger solder ball pad.

	SMD	NSMD
DOE1		
DOE2		
DOE3		
DOE4		

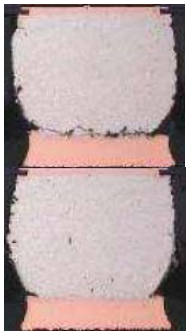
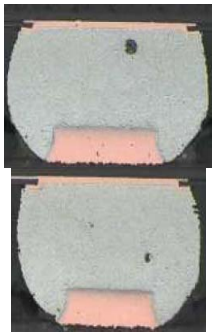
DOE5		

Figure 7. Optical micrographs of failure of DOE 1~5 samples.

In this study, both DOE 4 and5 UBM samples showed lower solder joint life cycle compared to non UBM samples. For UBM samples, SMD of DOE 4 and5 showed solder fatigue failure in board side as shown in Fig. 7 but NSDM of DOE 4 and 5 did not have major solder fatigue cracks. After further failure analysis of SEM micrographs, the Cu metal pad was observed as broken in conventional WLCSP [17,18,19].

In general, the reliability of WLCSP is dependant of a range of various design factors, for example:

- Dielectric materials property
- Dielectrics thickness
- UBM pad size/thickness
- Cu pad size/ Cu RDL thickness
- Cu pad opening size/Pad overlap size
- Solder materials / Solder ball size

In order to change failure mode from this to solder fatigue failure, those design parameters above are to be optimized based on thermo-mechanical simulation works in the future.

(a) (b)

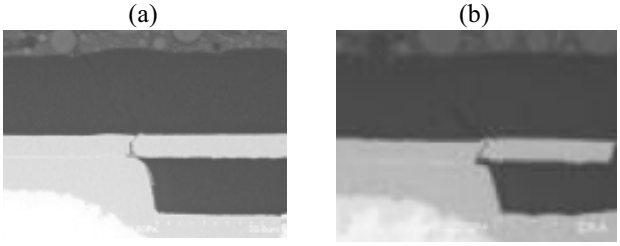


Figure 8 . SEM micrographs of failure of DOE 4 (with UBM & NSMD)

(a) (b)

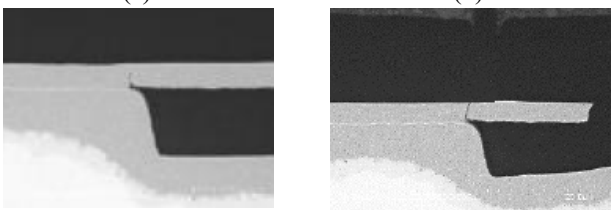


Figure 9. SEM micrographs of failure of DOE 5 (with UBM and solder alloy B & NSMD)

III. CONCLUSION

Thanks to its unique materials properties and thin film RLD with encapsulated structure, eWLB technology is an important wafer-level packaging solution that will enable the next-generation of automotive radar applications with its unique superior mmWave high frequency electrical performance. In this study, 9x9mm eWLB reliability was researched on component level and TCoB board level reliability with comprehensive DOE studies. The 9x9mm eWLB passed both AEC-Q100 Grade-1 package level reliability as well as TCoB board level reliability. To investigate dominating design factors for an improvement of TCoB performance, several DOEs were studied with experimental tests.

It was observed that the PCB pad structure and NSMD pads (versus SMD) changed solder fatigue mode, thereby improving the solder joint reliability. FA results showed solder fatigue failure for samples without UBM, but broken metal RDL was observed for samples with UBM samples corresponding to lower solder joint life cycle.

Furthermore, factors such as superior high frequency electrical performance in mmWave range and ability for heterogeneous integration; to integrate passives like inductors/resistor/capacitor into the various thin-film layers, active/passive devices into the mold compound or encapsulation, and achieve 3D vertical interconnections for new 3D SiP and 2.5D/3D packaging solutions, differentiate eWLB from other packaging technologies. eWLB technology provides a more holistic performance, and has potential to be a new packaging platform that widen its application to automotive, 5G and mmWave applications, such as antenna on package (AoP) or antenna in package (AiP).

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